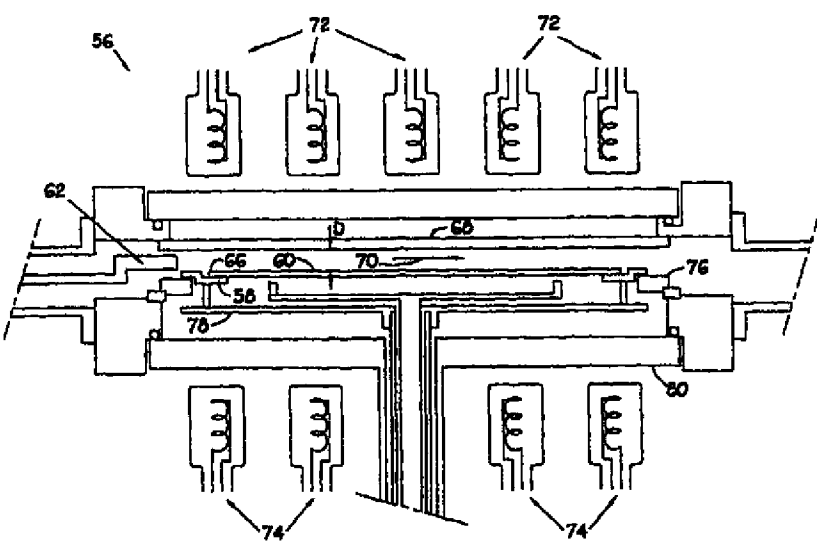


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(54) Title: HIGH RATE SILICON DEPOSITION METHOD AT LOW PRESSURES  (57) Abstract A method for high rate silicon deposition at low pressures, including a method of operating a CVD reactor (56) having a high degree of temperature and gas flow uniformity, the method of operation providing a combination of water temperature, gas flow and chamber pressure. According to the method, a substrate (60) is placed in a vacuum chamber wherein a reactant gas is provided at a high velocity in parallel with the substrate via a plurality of temperature controlled gas injectors (64) providing a condition wherein the deposition rate is only limited by the rate of delivery of unreacted gas to the substrate surface and the rate or removal of reaction byproducts. The combination of process conditions moves the reaction at the wafer surface into the regime where the deposition rate exceeds the crystallization rate, resulting in very small crystal growth and therefore a very smooth polysilicon film with a surface roughness on the order of 5-7 nm for films 2500 angstroms thick.		

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HIGH RATE SILICON DEPOSITION METHOD AT LOW PRESSURES

1 BACKGROUND OF THE INVENTION2 FIELD OF THE INVENTION

3 The present invention relates generally to methods for
4 chemical vapor deposition (CVD) of undoped and doped silicon,
5 and more particularly to a method for CVD of undoped and doped
6 silicon employing a novel combination of flow rate,
7 temperature and pressure to achieve improved film properties
8 at a high rate of deposition at low pressure.

9

10 BRIEF DESCRIPTION OF THE PRIOR ART

11 Amorphous, polycrystalline and epitaxial silicon are used
12 in the manufacturing of semiconductor devices and deposited
13 onto substrates (i.e. wafers) by chemical vapor deposition.
14 Such processes are carried out in a variety of commercially
15 available hot wall and cold wall reactors. Deposition is
16 accomplished by placing a substrate in a vacuum chamber,
17 heating the substrate and introducing silane or any similar
18 precursor such as disilane, dichlorosilane, silicon
19 tetrachloride and the like, with or without other gases.
20 Deposition rates of approximately 30 to 200 angstroms per
21 minute are achieved for low pressure processes (less than 1
22 Torr) as described in "Polycrystalline Silicon for Integrated
23 Circuit Applications" (T. Kamins, Kluwer Academic Publishers,
24 1988, p. 29). There are also some high pressure processes
25 available (25 to 350 Torr) that can achieve deposition rates
26 up to about 3,000 angstroms per minute as described in detail
27 in United States Patent Numbers 5,576,059 and 5,607,724 and
28 5,614,257.

29 A typical prior art vertical furnace low pressure
30 chemical vapor deposition (LPCVD) system is depicted in Fig. 1
31 and includes a chamber consisting of a quartz tube 10 and
32 chamber seal plate 12 into which is inserted a boat 14 for

1 carrying a plurality of substrates 16. Silane or other
2 similar precursor and a carrier gas such as hydrogen and a
3 dopant gas such as phosphine enter the gas injection tube (or
4 tubes) 18 from the gas inlet tube (or tubes) 20 through the
5 chamber seal plate 12. The gases exit the process chamber
6 through the seal plate 12 and out the exhaust port 24. A
7 plurality of heater elements 26 are separately controlled and
8 adjustable to compensate for the well-known depletion of the
9 feed gas concentration as the gas flows from the gas injection
10 tube 18 to the chamber exhaust port 24. This type of
11 deposition system typically operates in the 200 mTorr to 500
12 mTorr range (200×10^{-3} Torr to 500×10^{-3} Torr). Operating at
13 this low partial pressure of silane, or other similar
14 precursor, results in low deposition rates of the typically 30
15 to 200 angstroms per minute for deposition of pure silicon,
16 and 5 to 30 angstroms per minute if a dopant gas is
17 introduced. Operation at higher concentrations of reactant
18 gases results in non-uniform deposition across the substrates
19 and great differences in the deposition rate from substrate to
20 substrate. Increased flow rates could improve the deposition
21 uniformity at higher pressures, however increased gas flow
22 increases the reactive gas pressure at the injection tube
23 holes causing gas phase nucleation resulting in particles
24 being deposited on the substrates. Other problems associated
25 with this reactor include film deposition on the interior
26 quartz tube 10 and gas injection tube 18. This unwanted
27 deposition decreases the partial pressure of the reactive feed
28 gas concentration near the surface of the substrate 16
29 resulting in a reduced deposition rate and potential
30 contamination caused when film deposited on the wall of tube
31 10 and injector tube 18 flakes off and deposits on the
32 substrates 16. Finally, to offset the depletion of the
33 reactive chemical species from the entrance to the exit of
34 this style reactor, a temperature gradient is determined

1 across the substrate load zone that gives a uniform deposition
2 rate profile. However, this creates a different problem
3 because, in the case of polysilicon deposition, the grain size
4 is temperature dependent, and this temperature gradient causes
5 the polysilicon grain size to vary across the load zone. This
6 variation in grain size from substrate to substrate within a
7 plurality of substrates can cause problems with subsequent -
8 patterning of the polysilicon and variations in the electrical
9 performance of integrated circuits.

10 Another prior art reactor is illustrated in Fig. 2 and
11 described in detail in U.S. Patent 5,108,792. A substrate 28
12 is placed on a rotating substrate carrier 30, enclosed in a
13 vacuum tight chamber having an upper quartz dome 32 and a
14 lower quartz dome 34 and associated chamber wall 36. The
15 substrate 28 is heated by upper lamps 38 and lower lamps 40.
16 Reactant gases are injected through gas input tube 42 and
17 exhausted through exhaust tube 44. This reactor overcomes
18 some of the limitations of the vertical furnace reactor of
19 Fig. 1. The reactor can be operated at higher pressures than
20 vertical LPCVD furnaces and does not have an injector tube and
21 its associated problems. The reactor construction and high
22 rate of deposition at high pressure (typically greater than 10
23 Torr) is explained in U.S. Patents 5,576,059 and 5,607,724 and
24 5,614,257.

25 Increased deposition rates result in higher machine
26 productivity and more importantly reduce the time the
27 substrates are exposed to high temperatures, i.e. $>600^{\circ}\text{C}$.
28 Reduced time at high temperatures is important during the
29 fabrication of semiconductor devices as the device sizes
30 become smaller. Elevated temperatures, i.e. $>600^{\circ}\text{C}$, for any
31 extended time cause unwanted changes in semiconductor device
32 structure. A disadvantage of the prior art high pressure
33 methods is that operating at high pressure can cause a gas

1 phase reaction which can produce particulate contamination on
2 the wafer.

3 U.S. Patent 5,551,985 by Brors et al. describes a CVD
4 reactor that provides improved uniformity in heating a wafer,
5 and a highly uniform gas flow across the surface of a wafer.
6 U.S. Patent Applications Serial Nos. 08/909,461 filed on
7 August 11, 1997, and 09/228,835 and 09/228,840 filed on -
8 January 12, 1999, the disclosures of which are incorporated
9 herein by reference, describe wafer chambers in which related
10 processes may also be used.

11

12 SUMMARY OF THE INVENTION

13 It is an object of the present invention to provide a
14 method of operating a CVD reactor that provides a further
15 improvement in uniform deposition of silicon.

16 It is a further object of the present invention to
17 provide a method of operating a CVD reactor that optimizes the
18 rate and uniformity of deposition of silicon.

19 It is a still further object of the present invention to
20 provide a method of operating a CVD reactor that results in a
21 high degree of uniformity in deposition from one run to
22 another.

23 Briefly, a preferred embodiment of the present invention
24 includes a method of operating a CVD reactor having a high
25 degree of temperature and gas flow uniformity, the method of
26 operation providing a novel combination of wafer temperature,
27 gas flow and chamber pressure. According to the method, a
28 wafer is placed in a vacuum chamber wherein a reactant gas
29 flow is directed in parallel with the wafer via a plurality of
30 temperature controlled gas injectors, at a selected velocity
31 causing the deposition rate to be limited only by the rate of
32 delivery of unreacted gas to the wafer surface and the rate of
33 removal of reaction byproducts. The novel combination of
34 process conditions moves the reaction at the wafer surface

1 into the regime where the deposition rate exceeds the
2 crystallization rate, resulting in very small crystal growth
3 and therefore a very smooth polysilicon film with a surface
4 roughness on the order of 5-7 nm for films 2500 angstroms
5 thick. The process is configured to operate below what is
6 known as the "transition" temperature, at which level each
7 layer of film is deposited in an amorphous form and then
8 crystallizes as the deposition proceeds because of the lower
9 energy of the polycrystalline structure. As a result, the
10 silicon film is crystalline near the interface between the
11 deposited material and the wafer surface, and amorphous near
12 the top surface of the deposited material, resulting in a much
13 smoother surface than can be achieved with prior art
14 commercial equipment.

15 An advantage of the present invention is that it results
16 in smoother deposited film surfaces.

17 A further advantage of the present invention is that it
18 provides a process resulting in improved uniformity in film
19 deposition from batch to batch.

20 A still further advantage of the present invention is
21 that it provides a method resulting in higher rate deposition
22 of silicon with improved film smoothness and reproducibility
23 between batches.

24

25 BRIEF DESCRIPTION OF THE DRAWINGS

26 Fig. 1 illustrates a multiple wafer stack prior art
27 reactor;

28 Fig. 2 illustrates a single wafer prior art reactor;

29 Fig. 3 is a flow chart illustrating the steps of the
30 preferred embodiment of the present invention;

31 Fig. 4 shows a reactor that can be used to implement the
32 method of the present invention;

33 Fig. 5 is a list of operating parameters according to the
34 present invention;

1 Fig. 6 is a graph of deposition rate vs temperature;
2 Fig. 7 is a graph of deposition rate vs pressure;
3 Fig. 8 is a graph of deposition rate vs silane flow;
4 Fig. 9 is a plot showing film thickness variations for a
5 number of wafers; and
6 Fig. 10 is a plot showing the variation in thickness for
7 each of a number of wafers, from an average value. —

8

9 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

10 The method of the present invention will now be described
11 in reference to the flow chart of Fig. 3. The process begins
12 by placing a wafer on a carrier in a deposition chamber 46,
13 for deposition of polysilicon and/or amorphous silicon. The
14 carrier is rotated (48) and heated (50). The order of steps
15 48 and 50 is not significant in that the rotation is for the
16 purpose of enhancing the uniformity of silicon deposition, and
17 may be initiated any time prior to the injection of reactant
18 gases and then maintained during the deposition. The wafer is
19 preferably heated as uniformly as possible, with heat sources
20 above, below and surrounding the edge of the wafer. The
21 temperature to which the wafer is heated is preferably below a
22 temperature known as the "transition" temperature, the
23 preferred temperature range for silicon deposition being
24 500°C-700°C. The transition temperature will be more fully
25 discussed in the following text of the specification.

26 When the wafer is at the desired temperature, the process
27 gas for silicon deposition is initiated (52). The gas
28 pressure in the chamber is maintained at a selected pressure
29 less than 3 Torr but preferably less than 1 Torr, and the gas
30 is preferably injected through a plurality of cooled injector
31 nozzles with injection ports in close proximity to the wafer
32 edge, the nozzles oriented so as to direct the flow parallel
33 and close to the wafer surface. The gas is controlled to flow
34 at a velocity in excess of 10 cm/second and preferably at

1 least 50 to 100 cm/second across the wafer surface in a narrow
2 space confined to the region from the wafer surface to a
3 maximum space above the wafer of $\frac{1}{2}$ " to $1\frac{1}{2}$ ". The benefits and
4 reasons for this will be fully explained in the following
5 text. The velocity of the gas should be sufficient to reduce
6 the gas residence time to less than 500 milliseconds and
7 preferably less than 200 milliseconds. Subsequent to
8 deposition, the gas is turned off and evacuated from the
9 chamber, the rotation is stopped, and the wafer removed (54).

10 The results achievable with the method of the present
11 invention as described above in reference to Fig. 3 represent
12 a major improvement in silicon deposition. The term silicon
13 deposition or silicon, etc., will be used in this disclosure
14 as a generic term to include polysilicon, amorphous silicon,
15 and silicon with doping material. As discussed in the section
16 on prior art, previous systems achieved high rates of silicon
17 deposition (1,000-3,000 Å/minute) by running chambers at
18 relatively high pressures, typically in excess of 10 Torr.
19 Silicon deposition occurring at such high pressures has the
20 disadvantage in that it can cause a gas phase reaction which
21 can produce particulate contamination on the wafer. A major
22 advantage of the present invention is that the method provides
23 a very high deposition rate at very low chamber pressures,
24 resulting in very smooth, uniform and consistent surfaces.
25 With the method of the present invention, deposition rates of
26 3,000 Å/minute are achieved at chamber pressures in the range
27 of 300-700 mTorr. Film uniformity is typically 1%, measured
28 between the center of a 200 mm diameter silicon wafer and a
29 point 3 mm from the edge of the wafer. The reasons for this
30 improved performance will now be described in detail,
31 referring to each of the critical parameters of pressure,
32 temperature and gas velocity.

33 In accordance with the present invention, a wafer/
34 substrate is placed on a rotatable carrier in a vacuum chamber

1 wherein a high velocity reactant gas for depositing silicon,
2 such as silane, and a dopant gas if required, enter the
3 reactor/chamber in relatively close proximity to the rotated,
4 heated wafer. The gas is injected across the wafer at a
5 velocity in excess of 10 cm/second and preferably 50 to 100
6 cm/second or more, and is confined to a very narrow region
7 above the wafer so as to maximize the gas concentration at the
8 wafer surface. According to the method, the reactant gas is
9 preferably confined to the region extending from the wafer
10 surface to $\frac{1}{2}$ ", but no more than $1\frac{1}{2}$ " above the wafer. The high
11 velocity gas stream passing across the wafer surface has the
12 effect of thinning what is known as a "boundary layer"
13 immediately above the wafer. The boundary layer is a region
14 wherein unwanted reaction by-products collect. This layer
15 normally slows the rate of incidence of reactant gas, and
16 thereby slows the rate of deposition. The high velocity gas
17 stream of the present invention sweeps out the unwanted by-
18 products, thinning the boundary layer, allowing a higher rate
19 of desired reactant gas to reach the wafer surface, i.e.,
20 resulting in a further increase in the relative concentration
21 of the desired reactant species and reduced incorporation of
22 unwanted reaction by-products in the deposited film.

23 The combination of elements of the method of the present
24 invention are selected to achieve a more uniform, smooth film.
25 For example, the rapid gas flow described above, in
26 combination with a chamber pressure of about 260 mTorr and a
27 process temperature about 650°C changes the character of the
28 deposition from that of the prior art, moving it into a regime
29 where the reaction is occurring below what is known as a
30 "transition" temperature where the deposition rate exceeds the
31 crystallization rate, providing the benefit of an unusually
32 small amount of crystal growth. The result is a very smooth
33 polysilicon film with a surface roughness on the order of 5-7
34 nm for films 2,500 Å thick. In contrast, the nominal surface

1 roughness using a conventional prior art method is
2 approximately 70 nm as noted in the book "Polycrystalline
3 Silicon for Integrated Circuit Applications" by Ted Kamins,
4 page 54.

5 The nature and background of the phenomenon known as the
6 "transition" temperature will now be described in further
7 detail, and how the method of the present invention provides
8 for operation in this region.

9 In prior art methods of chemical vapor deposition (CVD)
10 of silicon, during the CVD deposition of silicon at a given
11 pressure, there is a transition temperature that when exceeded
12 will deposit a polycrystalline structure as the deposition
13 proceeds. In such a case, the underlying silicon atoms are
14 unlikely to continue rearranging after they have been covered
15 by further layers of deposited silicon atoms. This is an
16 undesirable result, causing a rough film surface. However, in
17 films deposited slightly below the transition temperature,
18 each layer of the film is deposited in an amorphous form and
19 crystallizes as the deposition proceeds because of the lower
20 energy of the polycrystalline structure. Nucleation of
21 crystallites is most likely to occur by heterogeneous
22 nucleation at the lower silicon-silicon dioxide interface.
23 Crystallization of the amorphous silicon proceeds from these
24 initial nuclei, with the crystalline region propagating upward
25 into the film by solid-phase epitaxial growth. When the
26 crystallization rate is less than the deposition rate, only
27 the lower portion of the film (starting from the silicon-
28 silicon dioxide interface) crystallizes during deposition,
29 even though the crystallization process continues during the
30 subsequent heating that occurs after the deposition is
31 terminated by shutting off the silane flow. Thus, the silicon
32 film can be crystalline near the interface and amorphous near
33 the top surface resulting in a very smooth surface texture
34 that is five to ten times smoother than the typical values

1 obtained from conventional polysilicon deposited films carried
2 out in presently available commercial equipment. Although it
3 is known that operation below the transition temperature can
4 result in a smooth film surface, prior art equipment and
5 methods do not allow such operation in a practical application
6 because the deposition rate is very slow. According to the
7 prior art, high deposition rates of 3,000 Å/minute are only
8 possible with chamber pressures above 10 Torr. In contrast,
9 the method of the present invention provides a combination of
10 elements, including rapid application of reactant gas and
11 removal of unwanted by-products, reducing the boundary layer,
12 operation between 500°C-700°C and at a pressure less than 3
13 Torr that results in operation below the transition
14 temperature at a very high deposition rate in a range
15 including 3,000 Å/minute. The non-uniformity of the deposited
16 silicon layer is less than 1.5%, measured between the center
17 of the wafer and a point 3mm from the edge of a 200 mm
18 diameter wafer. The surface roughness is in the order of 5-7
19 nm for a film 2,500 Å thick, deposited at a chamber pressure
20 of 1 Torr or less.

21 The development of the method of the present invention
22 was accomplished through use of a reactor similar to that
23 shown in the cross-sectional view of Fig. 4. The structure of
24 this apparatus is described in detail in U.S. Patent
25 5,551,985. According to the method, a reactant gas is
26 injected in close proximity to the edge of the wafer, and
27 directed across and parallel to the wafer surface at a high
28 velocity, confined to a narrow region above the wafer. Fig. 4
29 shows a reactor 56 having a rotatable susceptor 58 upon which
30 is placed a wafer 60. A gas injector apparatus 62 including a
31 plurality of nozzles with jets/openings 64, is positioned in
32 close proximity to the wafer edge 66, and is oriented to
33 direct a flow of reactant gas across and parallel to the wafer
34 60. The gas is further confined to a narrow region of width D

1 above the wafer surface by a thermal plate 68 positioned over
2 the wafer. By experiments with the positioning of plate 68,
3 it was determined that the optimum gap D lies between $\frac{1}{8}$ " and
4 $1\frac{1}{2}$ ". Similarly by experiment, the speed of gas flow from
5 injector 62 across the wafer was found to optimally exceed 50
6 to 100 cm/second in the direction indicated by arrow 70, for
7 the purposes of optimum reactant gas supply to the wafer
8 surface and removal of reaction by-products according to the
9 method described above.

10 According to the order of operations described in
11 reference to Fig. 1, the substrate/wafer 60 is first placed on
12 a carrier 58 and then brought to an operating temperature
13 between 500°C and 700°C. Typically, the apparatus of Fig. 1
14 can reach the temperature in about 20 seconds. The apparatus
15 as shown in Fig. 4 includes heaters 72 above, 74 below, and a
16 heat block 76 surrounding the carrier. This combination
17 provides uniform heating of the wafer 60. The carrier is then
18 rotated at a speed of approximately 5 RPM, and the reactant
19 gas is injected. The method of the present invention
20 minimizes deposition on chamber surfaces by specifying that
21 the reactant gas be confined to a narrow region above the
22 substrate. The apparatus of Fig. 4 further assists in this
23 objective by blocking reactant gas from passing underneath the
24 substrate. This is accomplished by injecting a non-reactive
25 gas (argon) at a low pressure under the substrate, between
26 thermal plate 78 and lower quartz window 80. The details of
27 the apparatus construction are fully described in U.S. Patent
28 5,551,985.

29 The preferred specifications for the method according to
30 the present invention are listed in Fig. 5, including a silane
31 flow rate in the range of 250-700 sccm, a chamber pressure in
32 the range of 200-750 mTorr, a gas velocity in excess of 100
33 cm/second confined to $\frac{1}{8}$ " over the wafer yielding a gas
34 residence time of less than 200 msec, a wafer uniformly heated

1 to a temperature in the range of 550°C-700°C, and wafer
2 rotation at a preferred rate of 5 RPM. Other rotation speeds
3 are also included in the spirit of the present invention.

4 Other factors that contribute to the performance of the
5 method applied to the apparatus of Fig. 4 include the
6 plurality of water-cooled injector nozzles, prevention of
7 reactant gas flow underneath the wafer, gas nozzles/jets
8 directed across and positioned close to the ends of the wafer,
9 and uniform wafer heating with heaters above, below, and
10 around the edge of the wafer.

11 Various performance factors are illustrated in the graphs
12 of Figs. 6-10. Fig. 6 shows the silicon deposition rate
13 versus wafer temperature with a chamber pressure of 250 mTorr.
14 It can be seen that the deposition rate is a rapid function of
15 temperature at 250 mTorr and therefore fairly critical. Fig.
16 7 shows the deposition rate versus chamber pressure at a
17 temperature of 650°C.

18 Fig. 8 shows the deposition rate as a function of silane
19 flow, which is proportional to the gas velocity over the
20 wafer.

21 Fig. 9 is a plot of the deposition thickness variation
22 within each wafer, for 25 wafers. The maximum film thickness
23 variation as shown is approximately 2.9%, with an average
24 variation around 1.5%.

25 Fig. 10 shows the variation in average film deposition
26 thickness from one wafer to another for 25 wafers. The
27 maximum deviation from the average for the batch is about 2%.

28 Although the present invention has been described above
29 in terms of a specific embodiment, it is anticipated that
30 alterations and modifications thereof will no doubt become
31 apparent to those skilled in the art. It is therefore
32 intended that the following claims be interpreted as covering
33 all such alterations and modifications as fall within the true
34 spirit and scope of the invention.

CLAIMS

- 1 1. A method of depositing silicon, comprising:
2 (a) placing a wafer on a carrier in a deposition
3 chamber;
4 (b) rotating said carrier;
5 (c) heating said wafer to a temperature of at least
6 500°C but below a transition temperature defined as a
7 temperature below which silicon will deposit in an amorphous
8 form;
9 (d) injecting a process gas for deposition of silicon
10 parallel to a surface of said wafer at a rate of at least 10
11 cm/sec; and
12 (e) maintaining a chamber pressure at a value less than
13 3 Torr.
- 1 2. A method as recited in claim 1 wherein said wafer is
2 heated to a temperature between 500°C and 700°C.
- 1 3. A method as recited in claim 1 wherein said velocity
2 is adjusted to cause an average gas residence time less than
3 500 milliseconds.
- 1 4. A method as recited in claim 1 wherein said process
2 gas is introduced into said chamber at a flow rate in the
3 range of 250 to 700 sccm.
- 1 5. A method as recited in claim 1 wherein said wafer is
2 heated to a temperature in the range of 650°C to 700°C.
- 1 6. A method as recited in claim 1 wherein said chamber
2 pressure is maintained in the range from 200-750 mTorr while
3 said process gas is being introduced into said chamber.

1 7. A method as recited in claim 1 wherein said process
2 gas is introduced to a plurality of gas nozzles in close
3 proximity to a wafer edge.

1 8. A method as recited in claim 1 wherein a dopant gas
2 is introduced to gas nozzles in close proximity to a wafer
3 edge.

1 9. A method as recited in claim 7 wherein said gas
2 nozzles are temperature-controlled.

1 10. A method as recited in claim 7 wherein said gas
2 nozzles are water-cooled.

1 11. A method as recited in claim 7 wherein said gas
2 nozzles are directed at a wafer surface.

1 12. An apparatus as recited in claim 7 wherein a
2 plurality of reactant gases enter through a plurality of
3 separate nozzles for each reactant gas.

1 13. A method as recited in claim 1 wherein the reactant
2 gas is confined to a narrow space above the wafer.

1 14. A method as recited in claim 11 wherein a distance
2 between the wafer and an upper heat shield is less than 1½".

1 15. A method as recited in claim 12 wherein a distance
2 between the wafer and an upper heat shield is less than 0.6".

1 16. A method as recited in claim 1 wherein the process
2 gas is prevented from passing below the wafer.

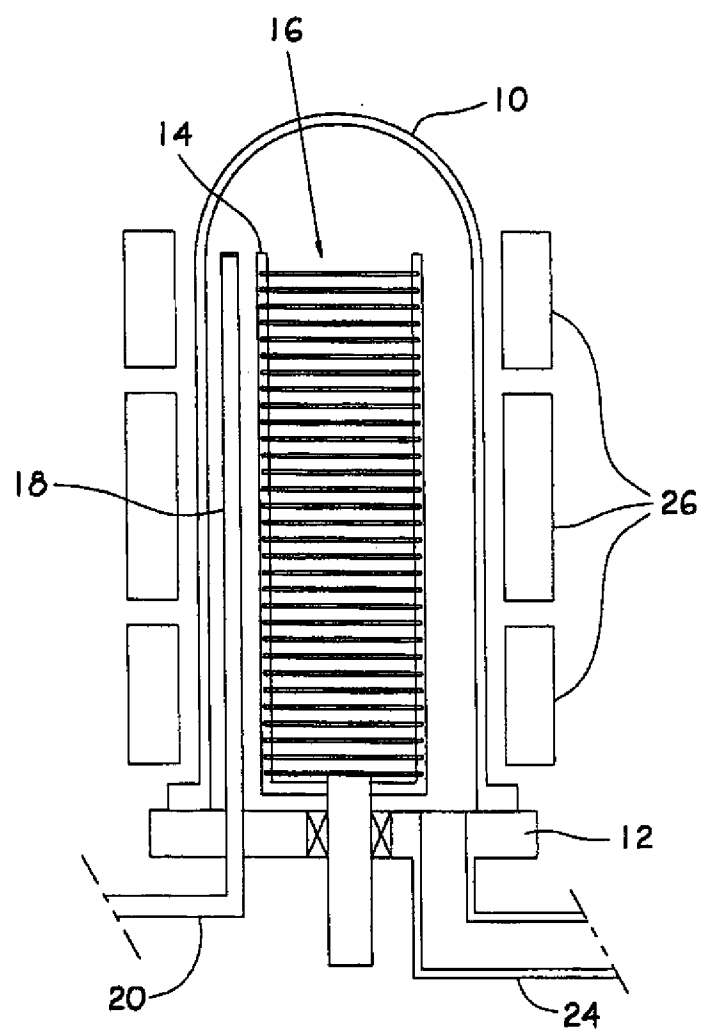


FIG. 1 (PRIOR ART)

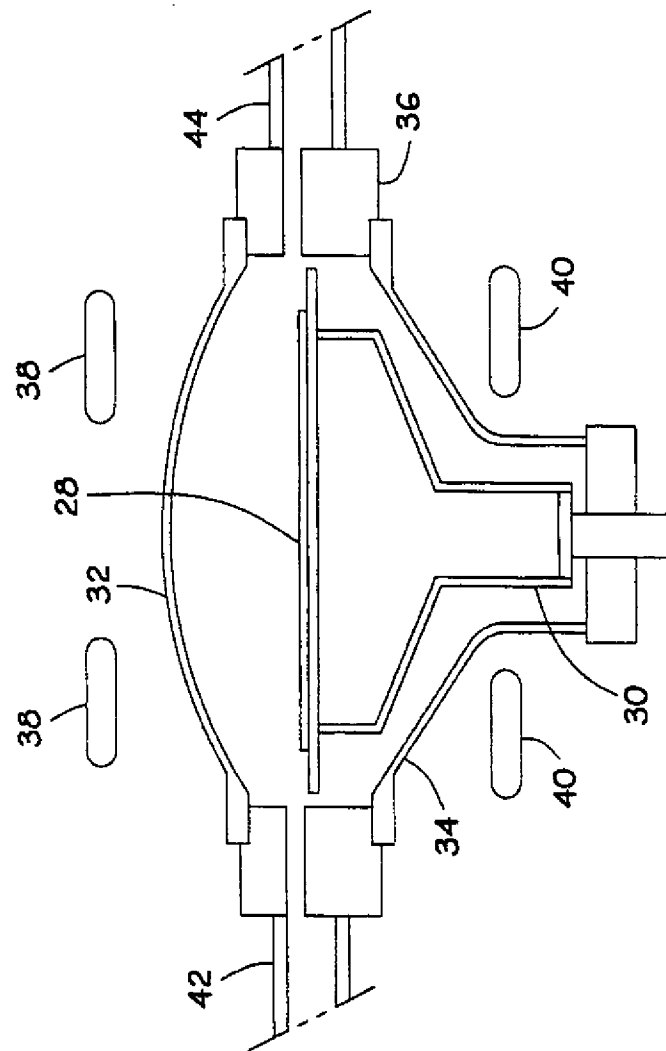


FIG. 2 (PRIOR ART)

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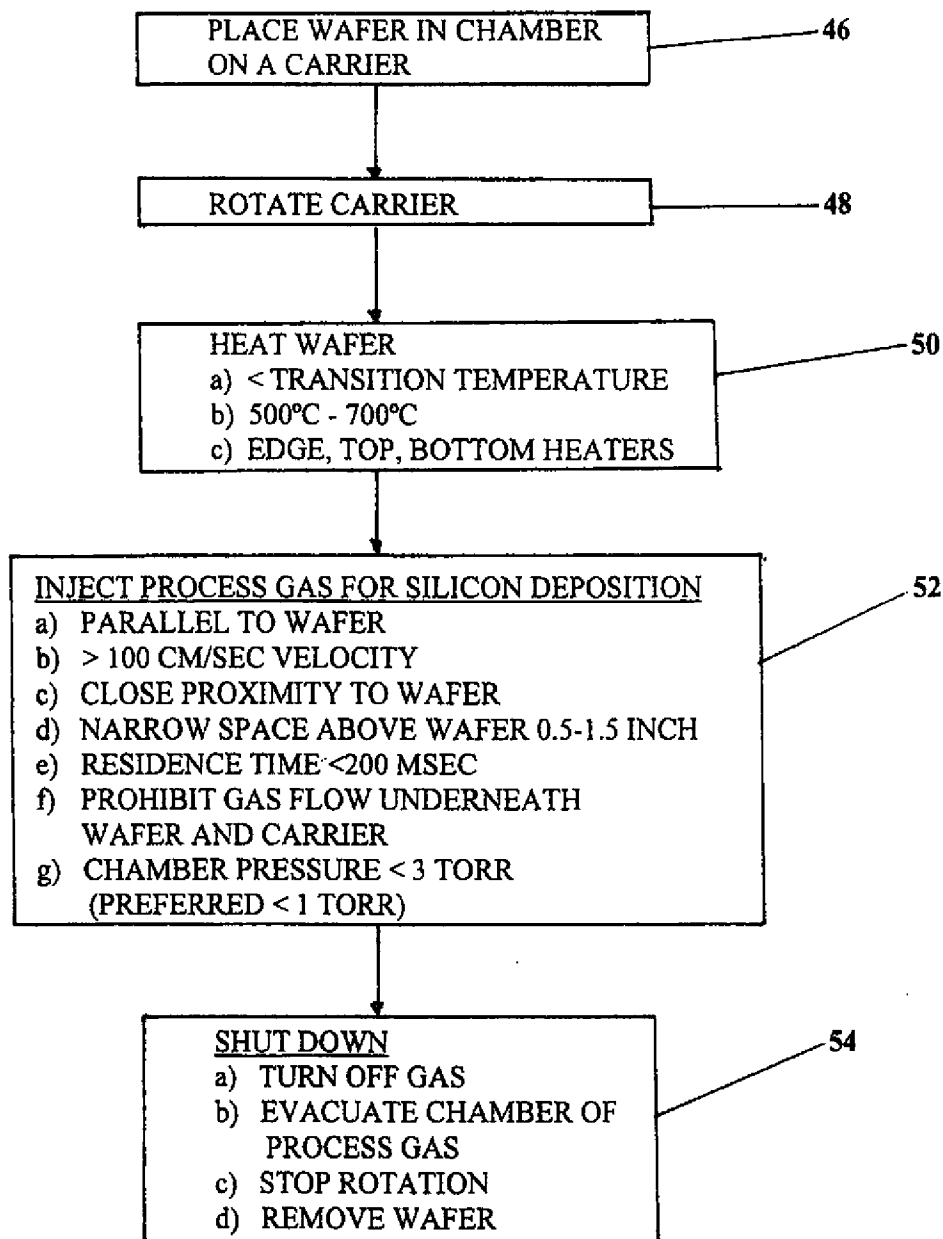


FIG. 3

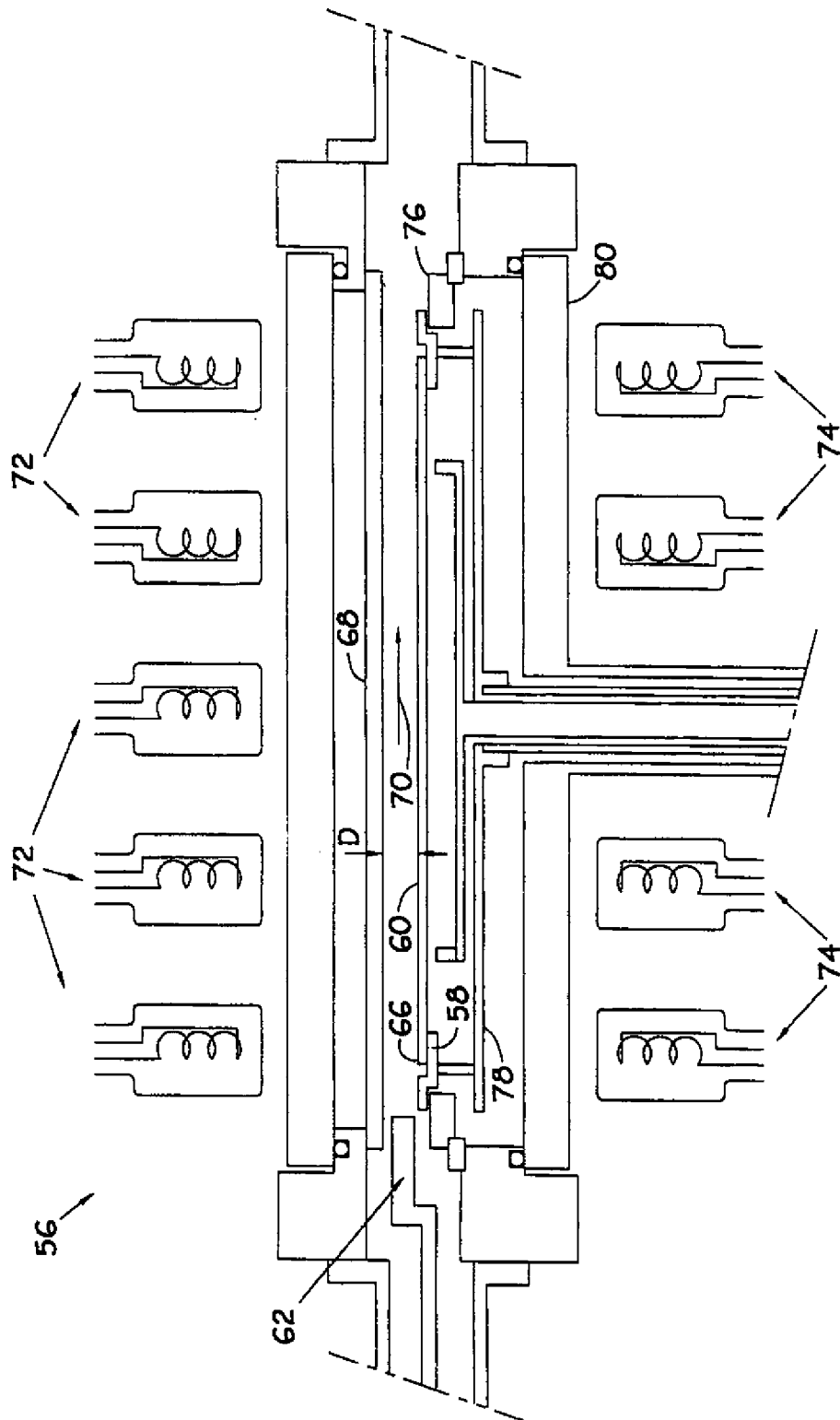


FIG. 4

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PROCESS SPECIFICATIONS

SILANE FLOW: 250 - 700 SCCM

CHAMBER PRESSURE: 200 - 750 mTORR

GAS VELOCITY: > 100 CM/SEC

WAFER TEMPERATURE: 550°C - 700°C

SUBSTRATE ROTATION: 5 RPM

6/10

Silicon Deposition Rate versus Temperature

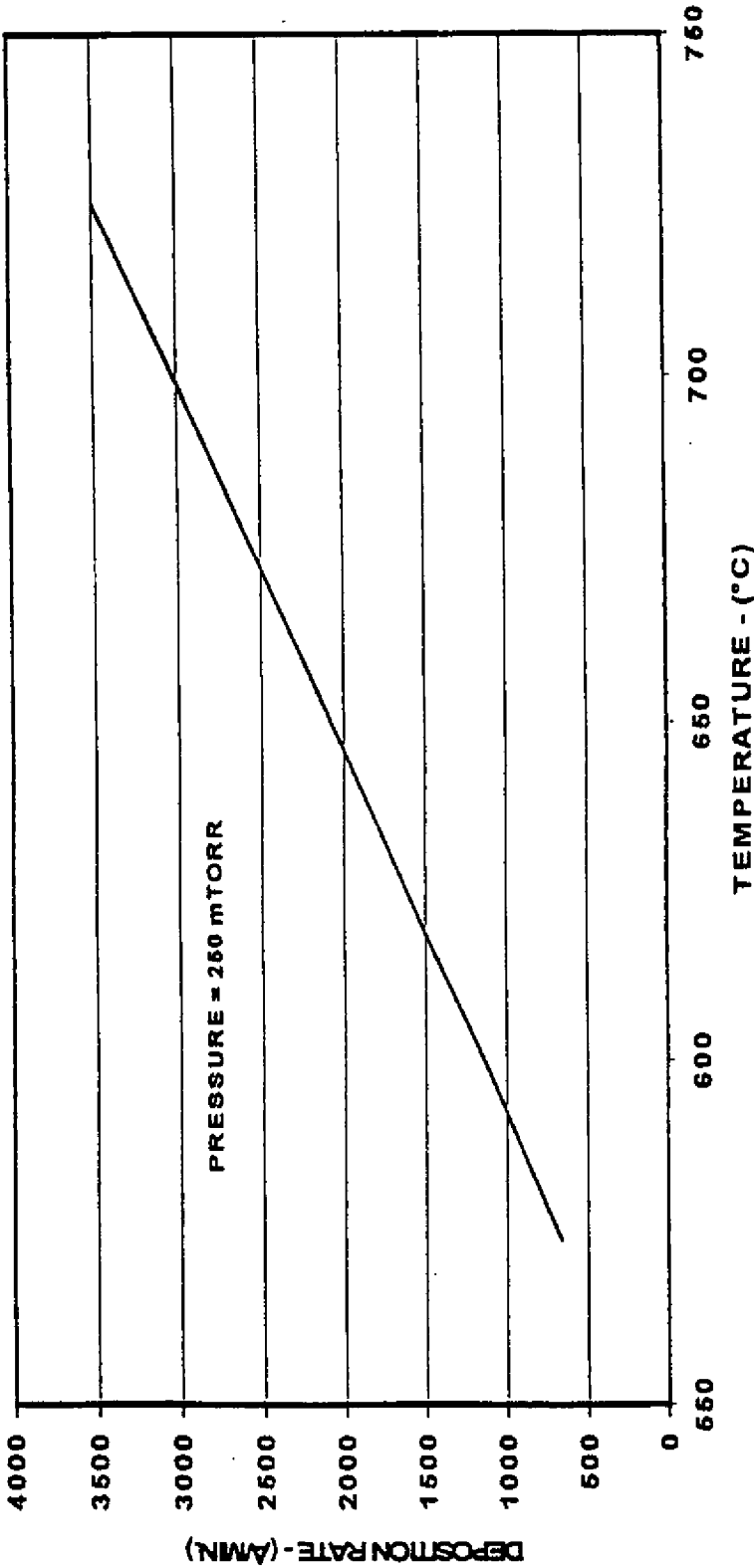


FIG. 6

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Silicon Deposition Rate versus Pressure

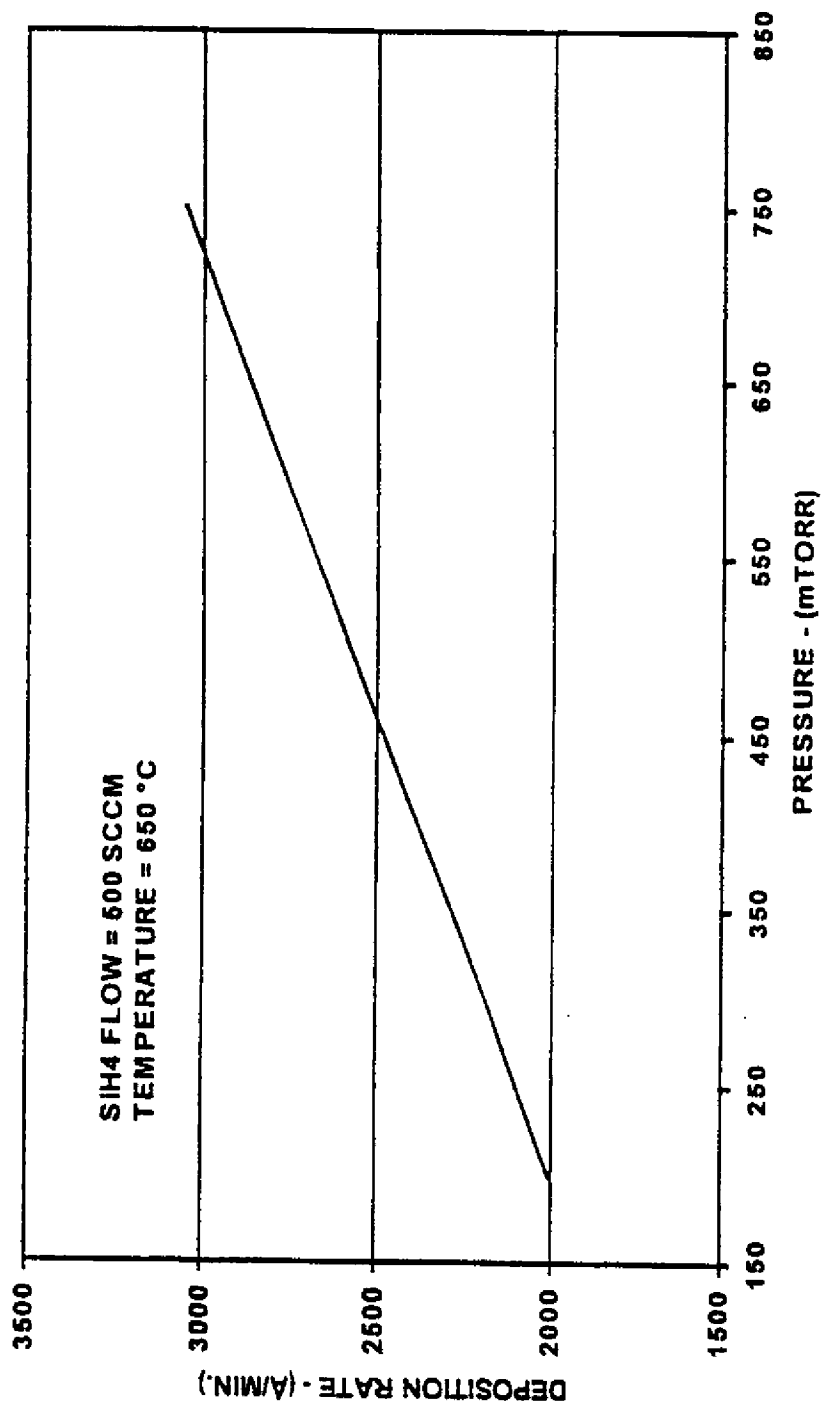


FIG. 7

Silicon Deposition Rate versus Silane Flow

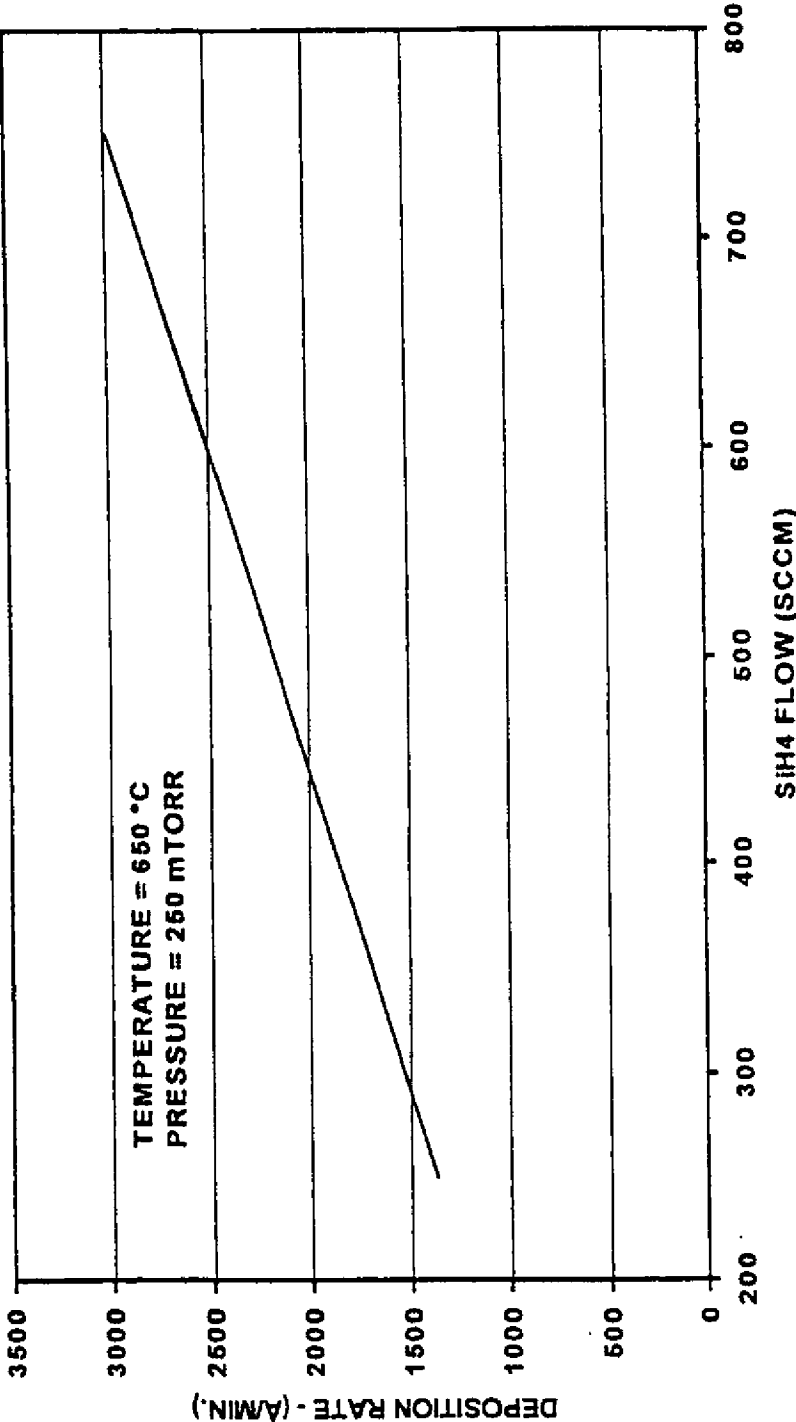


FIG. 8

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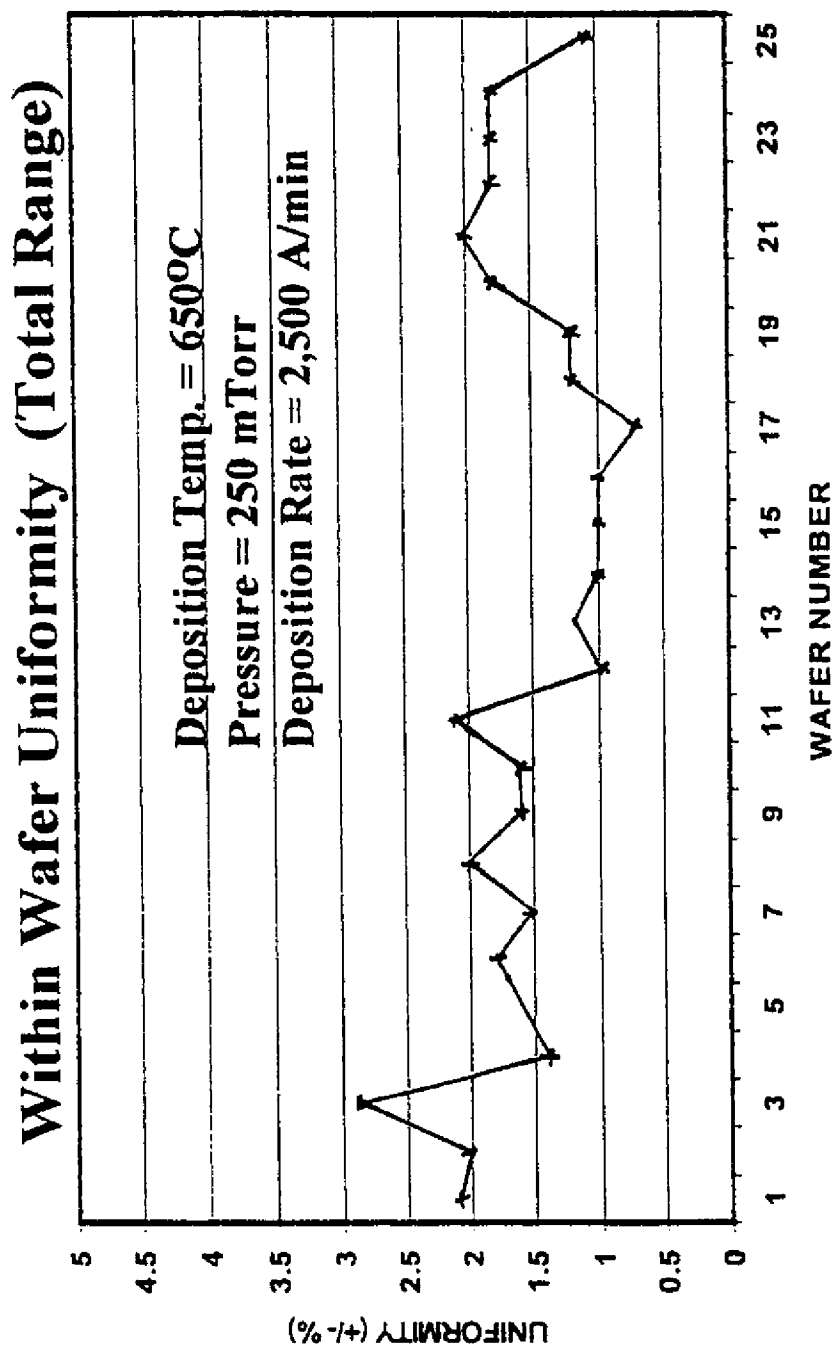


FIG. 9

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Run to Run Reproducibility

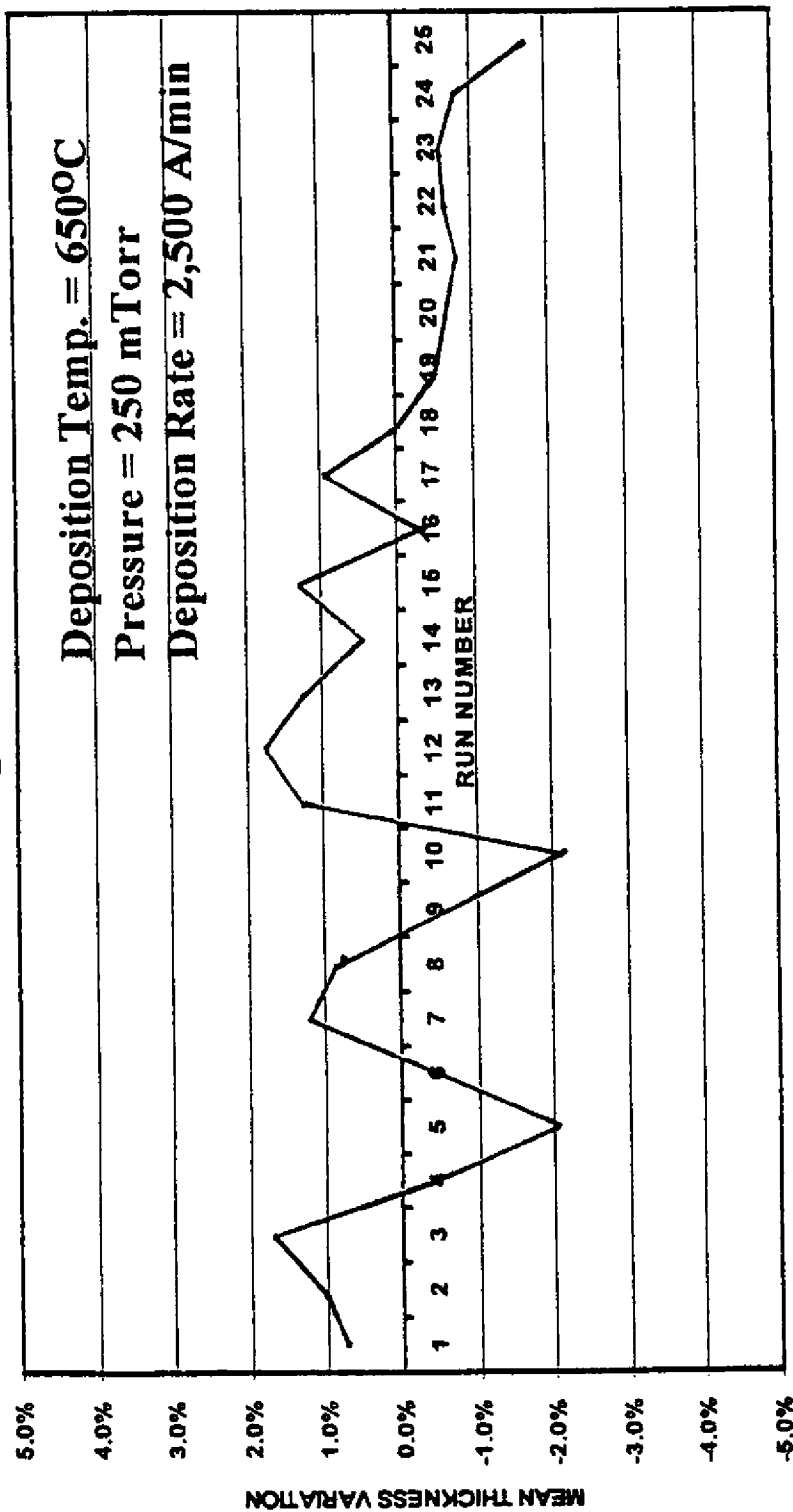


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/21200

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :C23C 16/24

US CL :438/680, 758; 427/578, 583, 255.18, 255.27, 255.393

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/680, 758; 427/578, 583, 255.18, 255.27, 255.393

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,976,996 A (MONKOWSKI et al) 11 December 1990, see Figure 1, col. 1, line 37, col. 4, lines 45-60, col. 6, lines 1-15, col. 7, lines 45-60, col. 9, lines 55-65.	1-16
Y	PIERSON, H. O., Handbook of Chemical Vapor Deposition, Noyes Publications, Park Ridge, New Jersey, USA, (1992), pages 184-185.	1-16

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*g* document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

03 DECEMBER 1999

Date of mailing of the international search report

19 JAN 2000

 Name and mailing address of the ISA/US
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